Manufacturing Processes for WSi$_2$-GPOSI Substrates and their Influence on Cross-talk Suppression and Inductance

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Introduction

The Performance of RF analogue ccts in Integrated Mixed signal Telecoms IC’s can be compromised by cross-talk through the silicon substrate from adjacent digital ccts.

• More severe as the frequency is increased especially in SOI

Solution: Integrate a WSi$_2$ ground plane to reduce the cross-talk.

Introduction of Ground plane makes integration of Inductors with high Q factor difficult.

• Image currents flowing in the ground plane.

Solution: Integration of solid and Patterned ground planes on one substrate.
OUTLINE

• QUB LPCVD of WSi\textsubscript{x}, x = 2.6
• GPSOI employing WSi\textsubscript{2} as the Ground Plane.
• WSi\textsubscript{2} and Cross-talk
  • Review test structure and initial results.(Pseudo SOI substrate)
  • Top-down GP contact and Faraday cage structures employing WSi\textsubscript{2}.
  • Effect of the WSi\textsubscript{2} Faraday Cage on Cross-talk
• WSi\textsubscript{2} Ground Planes and Inductors
  • Solid Ground Plane(SGP) Vs Patterned Ground Plane(PGP)
  • Inclusion of PGP structure into SOI.
Process Conditions

- **Gas Flow:** SiH$_4$ 200 sccm, WF$_6$ 3 sccm, Ar 200 sccm
- **Process Pressure:** 300mTorr
- **Temperature:** 370 °C
- **Deposition Rate:** 9.8 $\Omega$/s
- **Post Anneal sheet resistance:** 2 $\Omega$/sq
- **Layer stable at T<1100 °C**
Production of Ground Plane SOI Employing WSi₂ as the Ground Plane

1. Diffused silicon handle substrate
2. Silicon Active layer
3. SiO₂ growth
4. Silicium deposition
5. Bonding and High Temp. Annealing (1050°C, 2 hrs)
6. Grinding and polishing to required GPSOI thickness

- WSi₂ deposition (0.25μm)
- LPCVD polysilicon 0.8μm
- CMP leaving 0.3μm layer
WSi$_2$ GPSOI Structures
For Crosstalk Studies
Cross-Talk Test Structure and Initial Results Review

- Frequency range of 500 MHz to 50 GHz
- Locally grounded substrate exhibited 20 dB improvement on previously reported substrates.
Top-Down Contact Structure employing WSi$_2$

Trench Refill Process
1. Sidewall oxidation (0.3 µm)
2. WSi$_2$ Deposition (0.25 µm)
3. Polysilicon deposition (2 µm)
SEM of WSi$_2$ Lined Trench
Faraday Cage Structure

- Tx and Rx isolated by Faraday Cage.
- Cage consists of WSi₂ lined polysilicon filled Trench.
- Top-Down Contact to WSi₂ GP
- Tx, Rx pads 50 x 50µm. Probe spacing : 100µm
Alternative Faraday Cage Structure

- WSi$_2$ lined trenches (0.25 µm)
- Trench width: 2 µm.
- Trenches surround Transmitter and Receiver.
- Trenches grounded to the buried GP
Cross-talk Results

- Tx/Rx distance: 100 µm
- SOI thickness: 2 µm
- At 1 GHz, 70 dB improvement over control SOI.
- At 5 GHz, 30 dB improvement with inclusion of faraday cage structure
Summary

- WSi₂ can readily be incorporated into standard SOI structures to form GPSOI structures.
- WSi₂ employed in trench refill encapsulating Tx and Rx in a metal cage.
- Applying WSi₂ GPSOI technology to Cross-Talk studies:
  - Reduction in noise due to GP alone.
  - Further noise reduction with the inclusion of faraday cage.
- At 1 GHz, 70 dB improvement in Noise Figure.
WSi$_2$ GPSOI Structures and Inductance
# Inductor Fabrication

<table>
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<tr>
<th>PROCESS</th>
<th>DESCRIPTION</th>
<th>LOT1</th>
<th>LOT2</th>
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<tr>
<td>Evap. Al</td>
<td>0.5µm</td>
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<td>Mask 1 (Underlay)</td>
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<td>Spin on glass</td>
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<tr>
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<td>1.2µm</td>
<td>1.8µm</td>
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<tr>
<td>Mask 3 (Inductor coil)</td>
<td>Wet etch Al</td>
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<td>Yes</td>
</tr>
<tr>
<td>N2/H2 anneal</td>
<td></td>
<td></td>
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### Lot 1:
1. Inductors fabricated on Teos on WSi GP.
2. Inductors fabricated on Teos on implanted silicon simulating a GP.

### Lot 2:
1. Inductors fabricated on Teos on silicon
2. Inductors fabricated on Teos on Patterned WSi GP
Spiral Inductor Structures

Inductor Dimensions

- Track Width: 12 µm
- Track Spacing: 6 µm
- No. Of Turns: 2, 3, 4, 5, 6, 7

4 Turn Octagonal Inductor  6 Turn Rectangular Inductor

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Comparison of Measured Inductance with Empirical Calculations

Mohan et al (IEEE Journal of solid state ccts Vol 34(10))

Present Two empirical formulae

**Modified Wheeler**

\[ L_{mwh} = K_1 \mu_0 \frac{n^2 \text{davg}}{1 + K_2 \rho} \]

**Current Sheet Approx**

\[ L_{csa} = \frac{\mu_0 n^2 \text{davg} c_1}{2} \left( \ln\left(\frac{c_2}{\rho}\right) + c_3 \rho + c_4 \rho^2 \right) \]

- \( n = \text{No. Turns} \)
- \( \rho \) (fill ratio) = (dout-din)/(dout+din)
- \( \text{davg} = 0.5(\text{dout+din}) \), \( \mu_0 \) = permeability of free space
- \( K_1,K_2,C_1-C_4 \) are geometry dependant constants
Spiral Inductors on PGP’S

Patterned Gnd Plane

Aluminium Underlay on PGP

Magnified Image of Aluminium Inductor on PGP
Comparison of Inductor Measurements for No GP, Diffused GP, SGP and PGP

W = 12 µm, S = 6 µm, n = 4

- Qmax reduces by 55% with inclusion of SGP
- L values effectively remain constant
- Introducing a PGP results in a slight improvement of Qmax
Incorporation of PGP into GPSOI

Integration of Patterned areas and solid areas on the same substrate.

**Planarisation Issue**
- Distance between two WSi₂ fingers must be less than 100 µm. In this case: 8 µm
- Polysilicon deposition
- Chemical mechanical polishing. - Producing surface suitable for bonding.


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Process Sequence for Incorporation of PGP and SGP on same substrate

1. LPCVD of WSi. Selective patterning of GP leaving PGP and SGP regions.
2. LPCVD of Polysilicon. (>0.8µm)
3. CMP of polysilicon leaving a planarised bondable surface. Polysilicon(0.2 µm).
4. Bonding of planarised polysilicon layer to oxidised active substrate.
5. Post bond Anneal 1050C 2 hrs
6. Grind and polish to required active layer thickness.
Conclusions

**GP PROCESS INTEGRATION**

- WSi$_2$ can be readily integrated into SOI process:
  - Require CMP of a Polysilicon layer.
  - Polysilicon to oxide bond
- For GPSOI substrates WSi$_2$ can be used in contact Via refill.

**GPSOI AND CROSS-TALK**

- Top-Down contact to GP using WSi$_2$ in Via refill.
- WSi$_2$ employed in Faraday cage structure creating an enclosed metal cage.
- GP greatly reduces noise between Tx and Rx.
  - At 1GHz 35dB improvement in noise for WSi$_2$ GP only, over control SOI.
  - At 1GHz 70dB reduction in noise for Faraday cage over the SOI control.
Conclusions

GPSOI AND INDUCTANCE

• Introduction of GP results in a reduction of inductor Quality Factor.
  • 55% reduction in Q.
• Employing a patterned GP structure results in no loss of inductor Quality Factor.
  • Slight improvement of Q.
• Integration of SGP and PGP on the same Die/Substrate requires trench refill and planarisation.