Manufacturing Processes for WSi_2-GPSOI Substrates and their Influence on Cross-talk Suppression and Inductance

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Introduction

The Performance of RF analogue ccts in Integrated Mixed signal Telecoms IC's can be compromised by cross-talk through the silicon substrate from adjacent digital ccts.

• More severe as the frequency is increased especially in SOI

Solution: Integrate a WSi_2 ground plane to reduce the cross-talk.

Introduction of Ground plane makes integration of Inductors with high Q factor difficult.

• Image currents flowing in the ground plane.

Solution: Integration of solid and Patterned ground planes on one substrate.

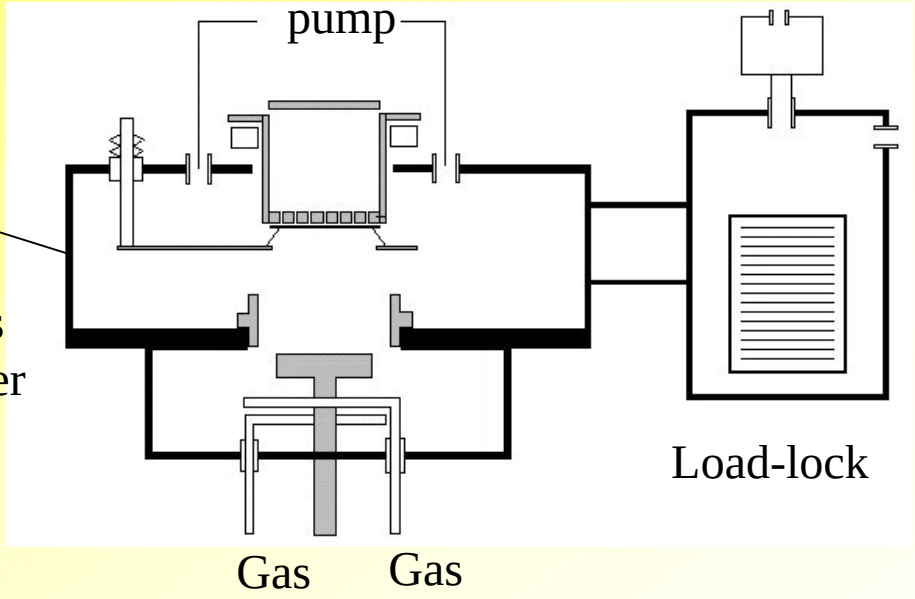
OUTLINE

- **QUB LPCVD of WSi_x, x = 2.6**
- **GPSOI employing WSi_2 as the Ground Plane.**
- **WSi_2 and Cross-talk**
  - Review test structure and initial results.(Pseudo SOI substrate)
  - Top-down GP contact and Faraday cage structures employing WSi_2.
  - Effect of the WSi_2 Faraday Cage on Cross-talk
- **WSi_2 Ground Planes and Inductors**
  - Solid Ground Plane(SGP) Vs Patterned Ground Plane(PGP)
  - Inclusion of PGP structure into SOI.

QUB LPCVD WSi_2

Process Conditions

- **Gas Flow: SiH_4 200 sccm,**
  WF_6 3 sccm,
  Ar 200 sccm
- **Process Pressure: 300mTorr**
- **Temperature: 370 °C**
- **Deposition Rate: 9.8 Å/s**
- **Post Anneal sheet resistance: 2 Ω/□**
- **Layer stable at T<1100 °C**



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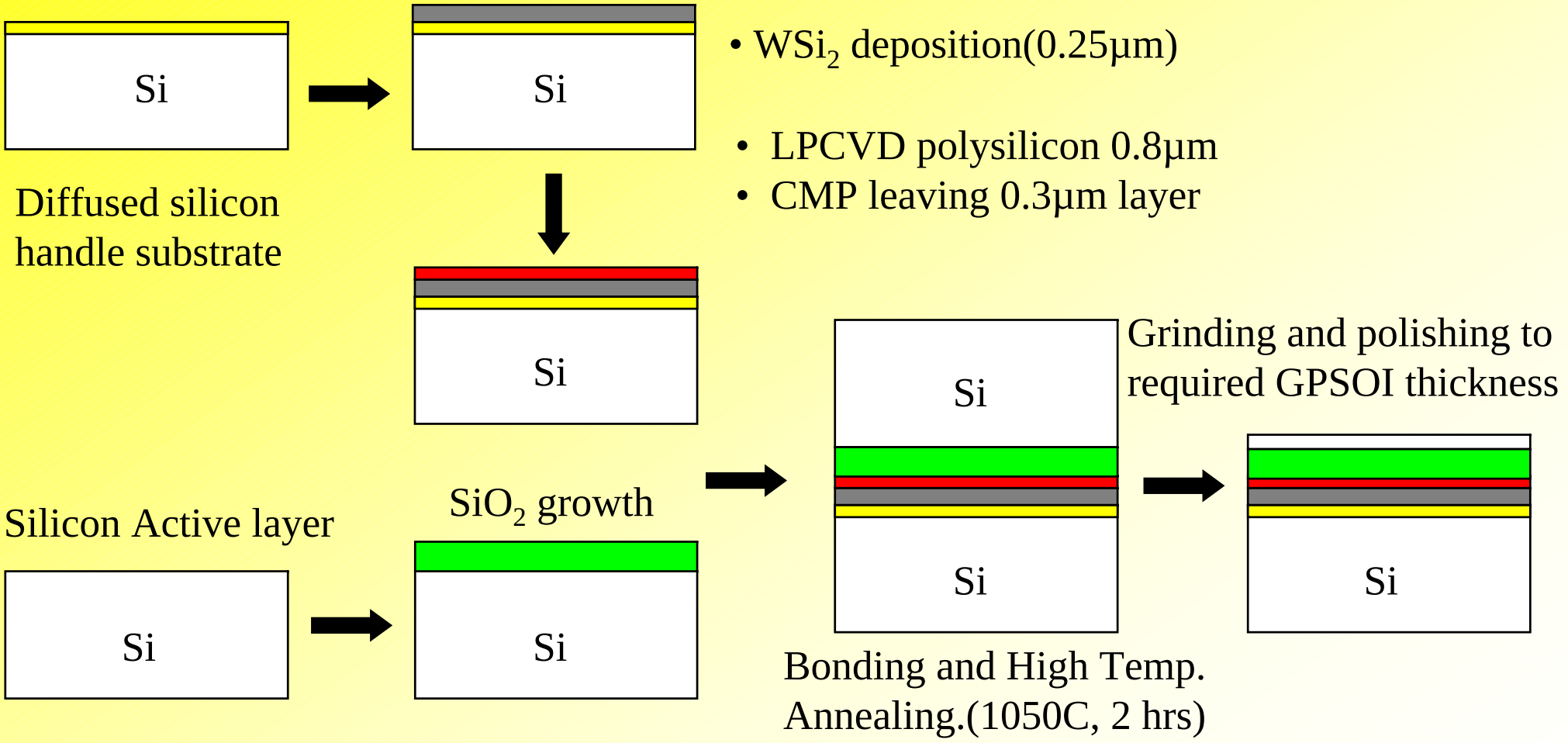
Production of Ground Plane SOI Employing WSi_2 as the Ground Plane



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WSi_2 GPSOI Structures For Crosstalk Studies

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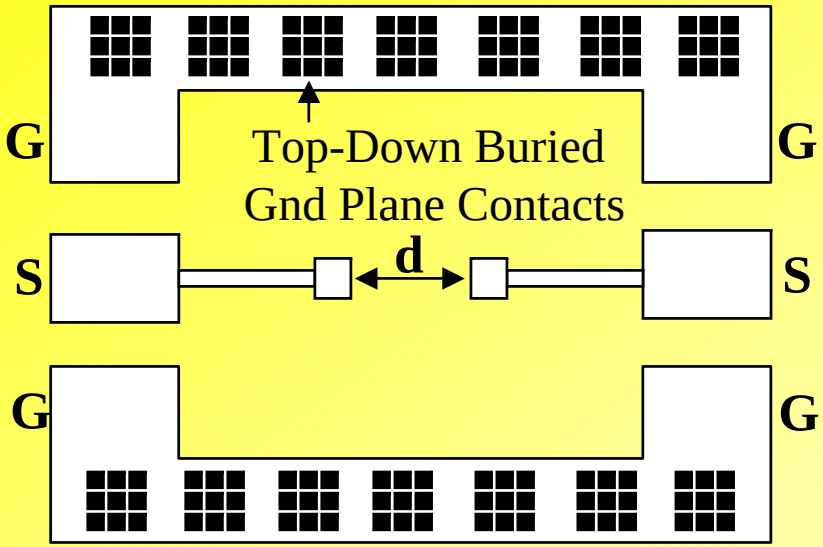
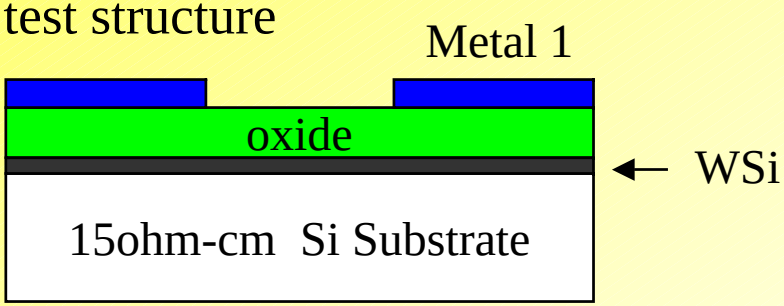
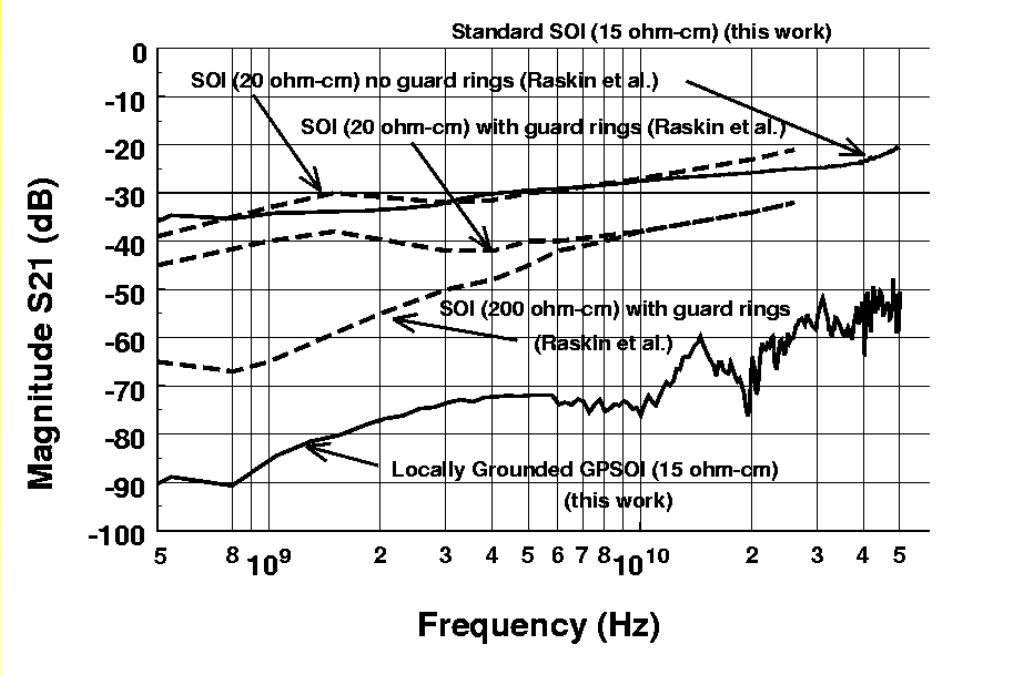
Cross-Talk Test Structure and Initial Results Review



Ground -Signal-Ground Co-Planar test structure





- Frequency range of 500 MHz to 50 GHz
- Locally grounded substrate exhibited 20 dB improvement on previously reported substrates.

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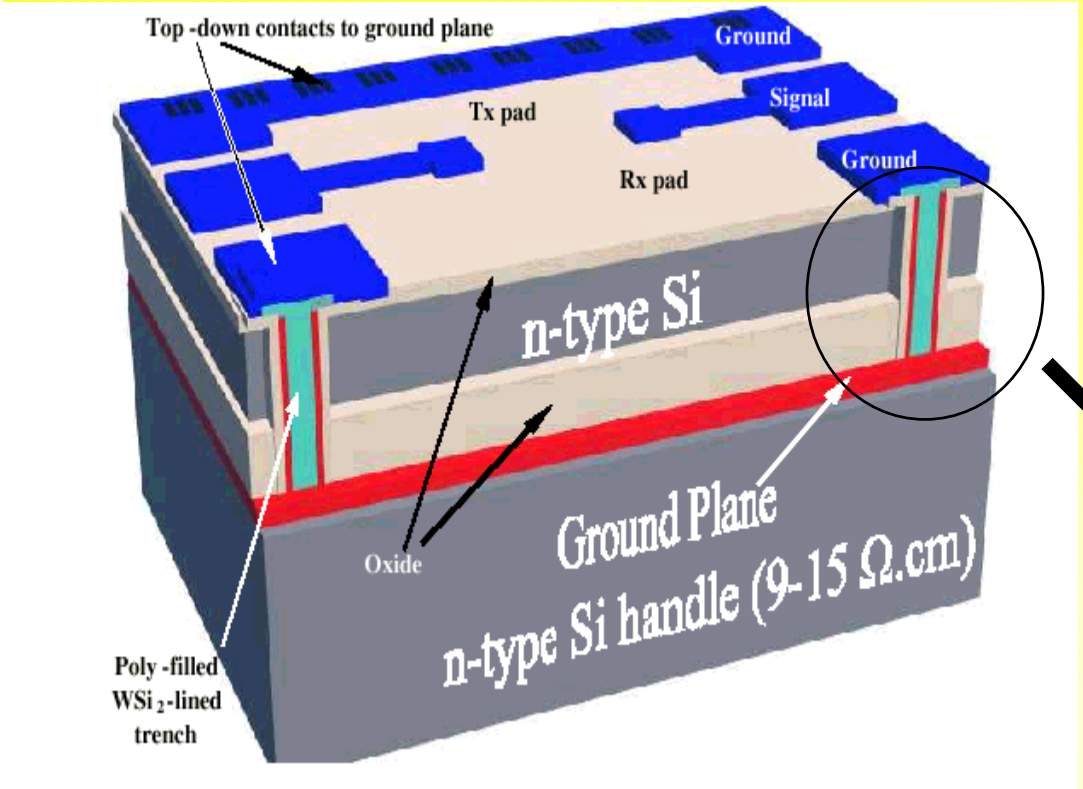
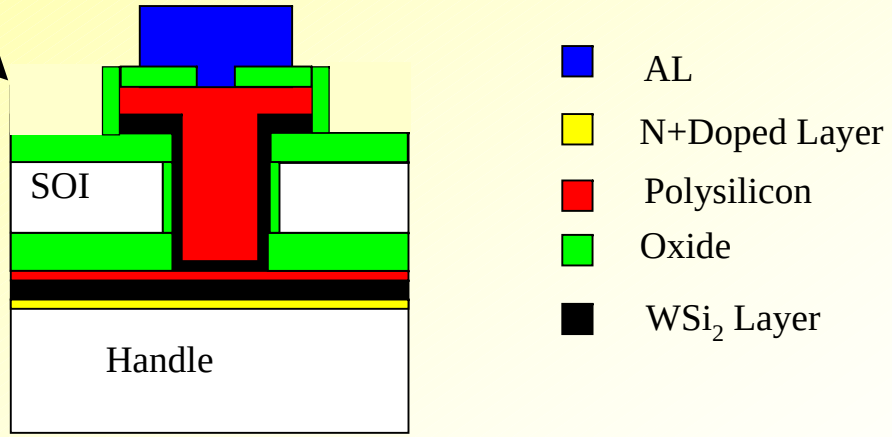
Top-Down Contact Structure employing WSi_2



Trench Refill Process

1. Sidewall oxidation (0.3 µm)
2. WSi_2 Deposition (0.25 µm)
3. Polysilicon deposition (2 µm)



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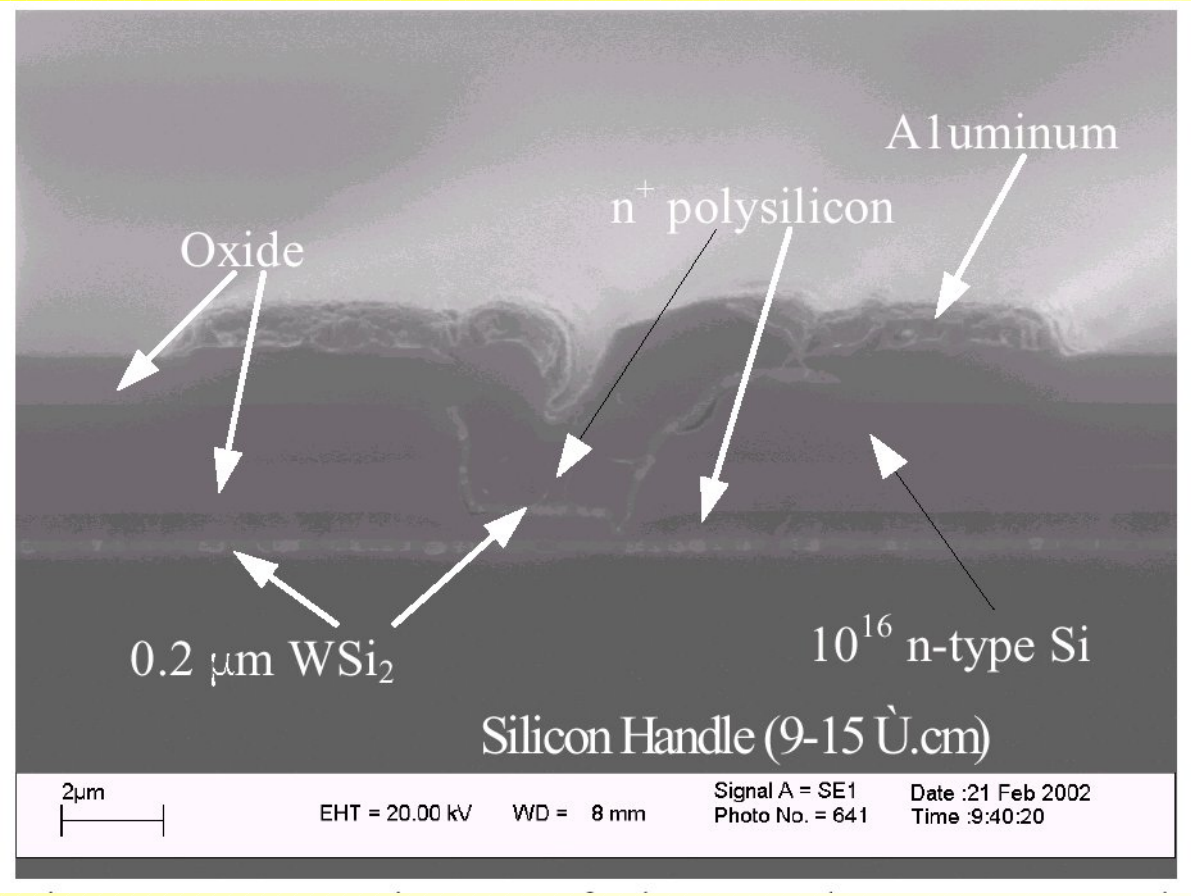
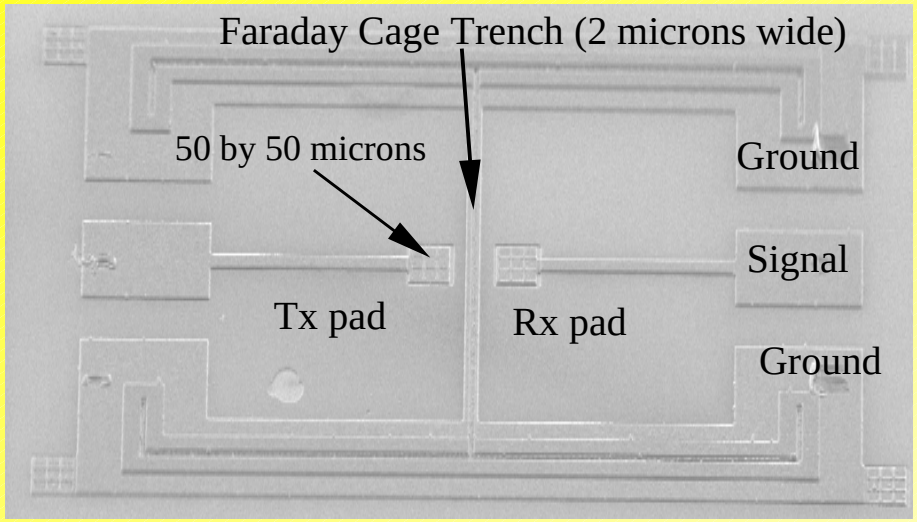
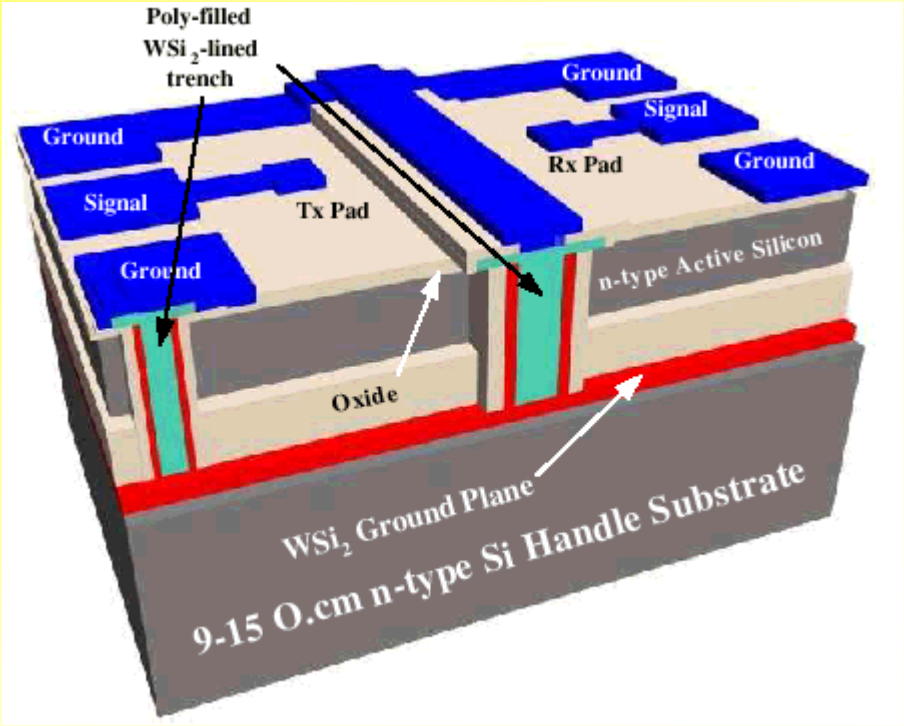
SEM of WSi_2 Lined Trench



Faraday Cage Structure





- Tx and Rx isolated by Faraday Cage.
- Cage consists of WSi_2 lined polysilicon filled Trench.
- Top-Down Contact to WSi_2 GP
- Tx, Rx pads 50 x 50µm. Probe spacing : 100µm

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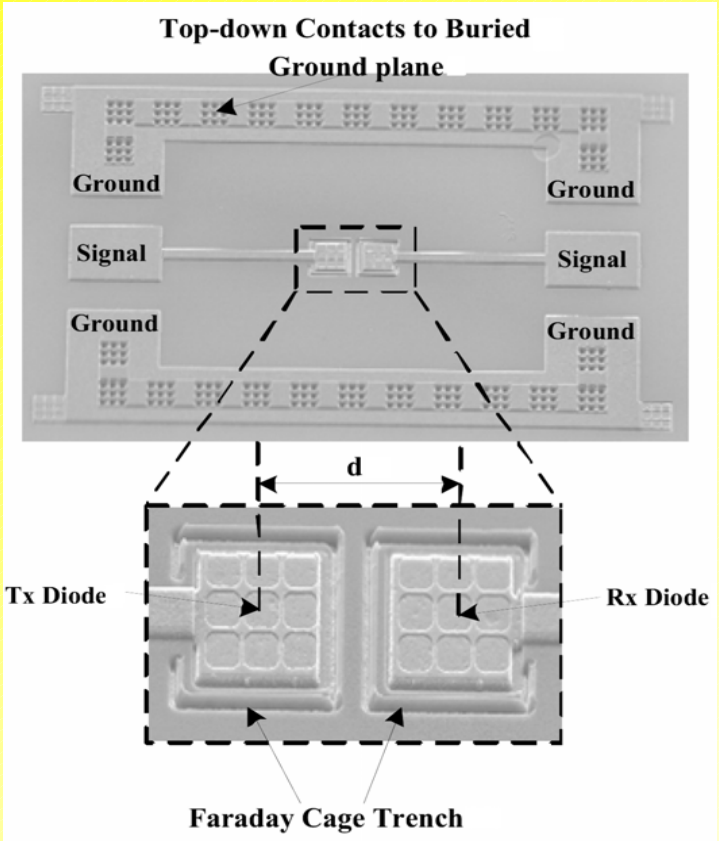
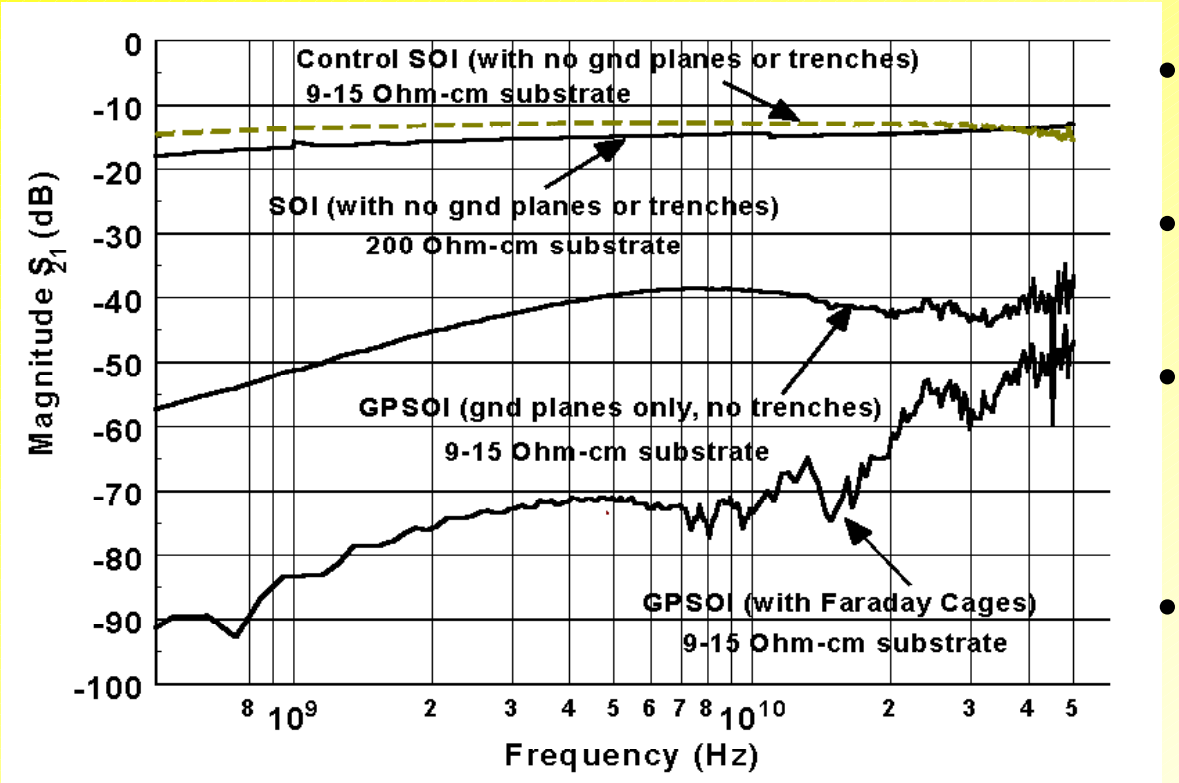
Alternative Faraday Cage Structure



- WSi_2 lined trenches (0.25 µm)
- Trench width: 2 µm.
- Trenches surround Transmitter and Receiver.
- Trenches grounded to the buried GP

Cross-talk Results



- Tx/Rx distance: 100 µm
- SOI thickness: 2 µm
- At 1 GHz, 70 dB improvement over control SOI.
- At 5 GHz, 30 dB improvement with inclusion of faraday cage structure

Summary

- WSi_2 can readily be incorporated into standard SOI structures to form GPSOI structures.
- WSi_2 employed in trench refill encapsulating Tx and Rx in a metal cage.
- Applying WSi_2 GPSOI technology to Cross-Talk studies:
    - Reduction in noise due to GP alone.
    - Further noise reduction with the inclusion of faraday cage.
- At 1 GHz, 70 dB improvement in Noise Figure.

WSi_2 GPSOI Structures and Inductance

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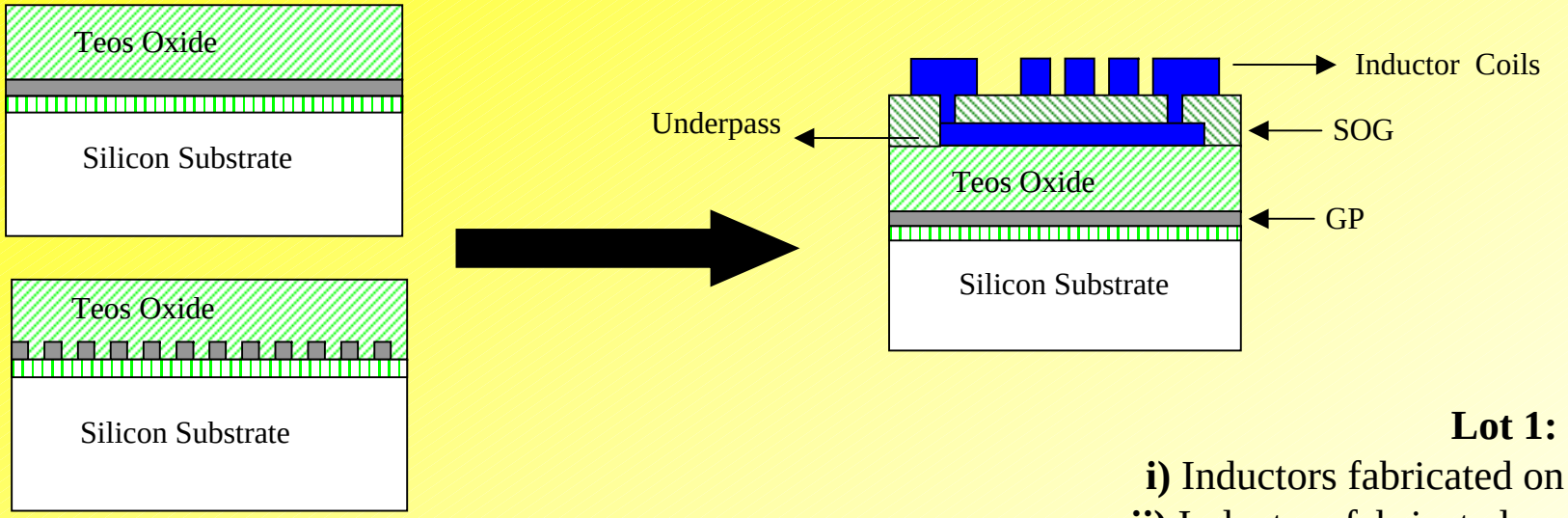
Inductor Fabrication



PROCESS	DESCRIPTION	LOT1	LOT2
Evap. Al	0.5µm	0.5µm	0.8µm
Mask 1(Underlay)	Wet etch Al	Yes	Yes
Spin on glass	0.6µm	0.6µm	0.6µm
Mask 2(Via)	BHF etch	Yes	Yes
Sputter Al	1.5µm	1.2µm	1.8µm
Mask 3 (Inductor coil)	Wet etch Al	Yes	Yes
N2/H2 anneal			

Lot 1:

i) Inductors fabricated on Teos on WSi GP.

ii) Inductors fabricated on Teos on implanted silicon simulating a GP.

Lot 2:

i) Inductors fabricated on Teos on silicon

ii) Inductors fabricated on Teos on Patterned WSi GP

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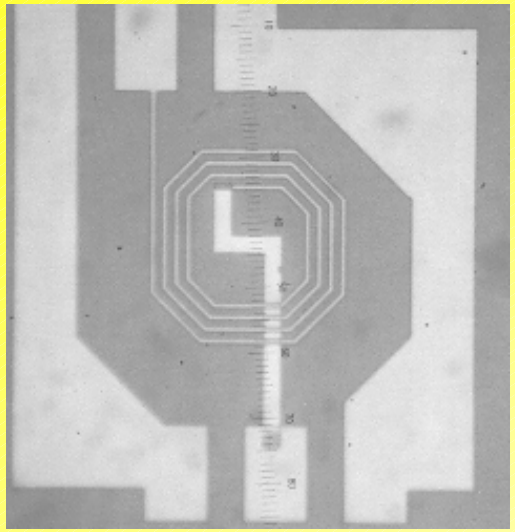
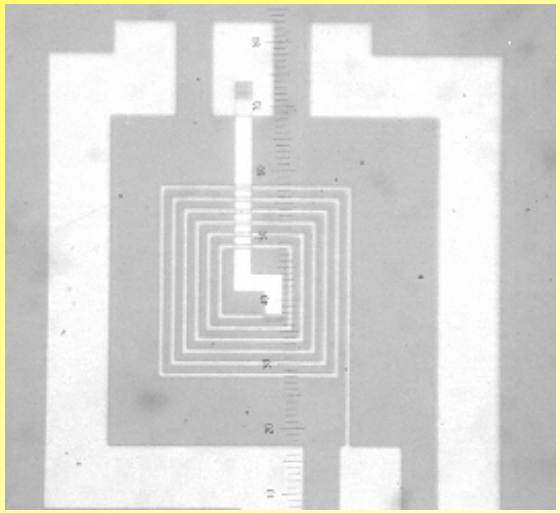
Spiral Inductor Structures



4 Turn Octagonal Inductor



6 Turn Rectangular Inductor

Inductor Dimensions

Track Width: 12 µm

Track Spacing: 6 µm

No. Of Turns: 2,3,4,5,6,7

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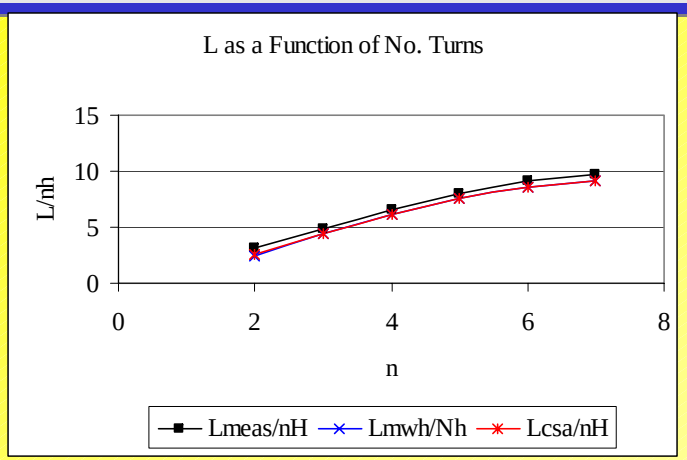
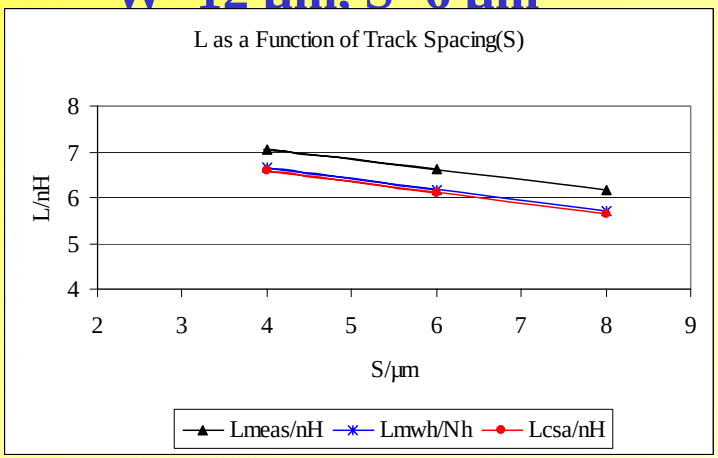
Comparison of Measured Inductance with Empirical Calculations



W=12 um, S=6 um



W=12 µm, N=4

Mohan et al(IEEE Journal of solid state ccts Vol 34(10))
Present Two empirical formulae

Modified Wheeler

$$Lmwh = K1\mu 0\frac{n^2 davg}{1+K2\rho}$$

Current Sheet Approx

$$L_{csa} = \frac{\mu_0 n^2 d_{avg} c_1}{2}\left(\ln\left(c_2/\rho\right)+c_3\rho+c_4\rho^2\right)$$

n = No. Turns ρ(fill ratio) = (dout-din)/(dout+din)
davg = 0.5(dout+din),μ_0 = permeability of free space
K1,K2,C1-C4 are geometry dependant constants

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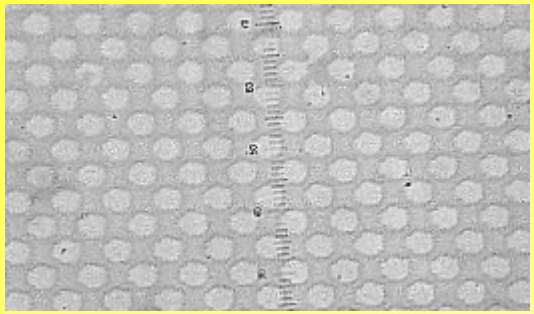
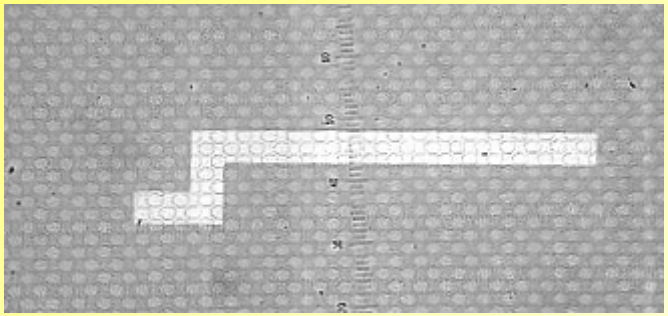
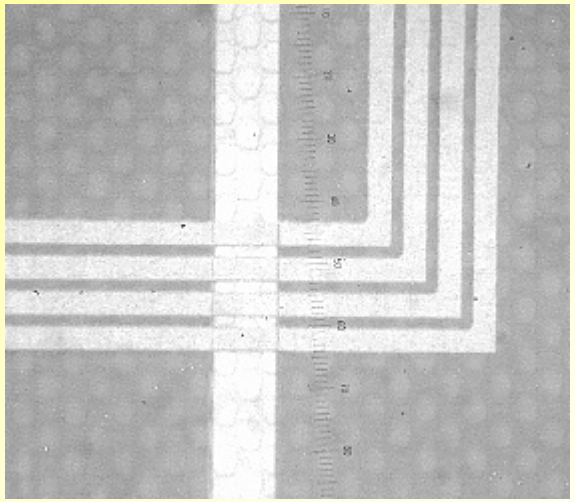
Spiral Inductors on PGP'S



Patterned Gnd Plane



Aluminium Underlay on PGP



Magnified Image of Aluminium Inductor on PGP

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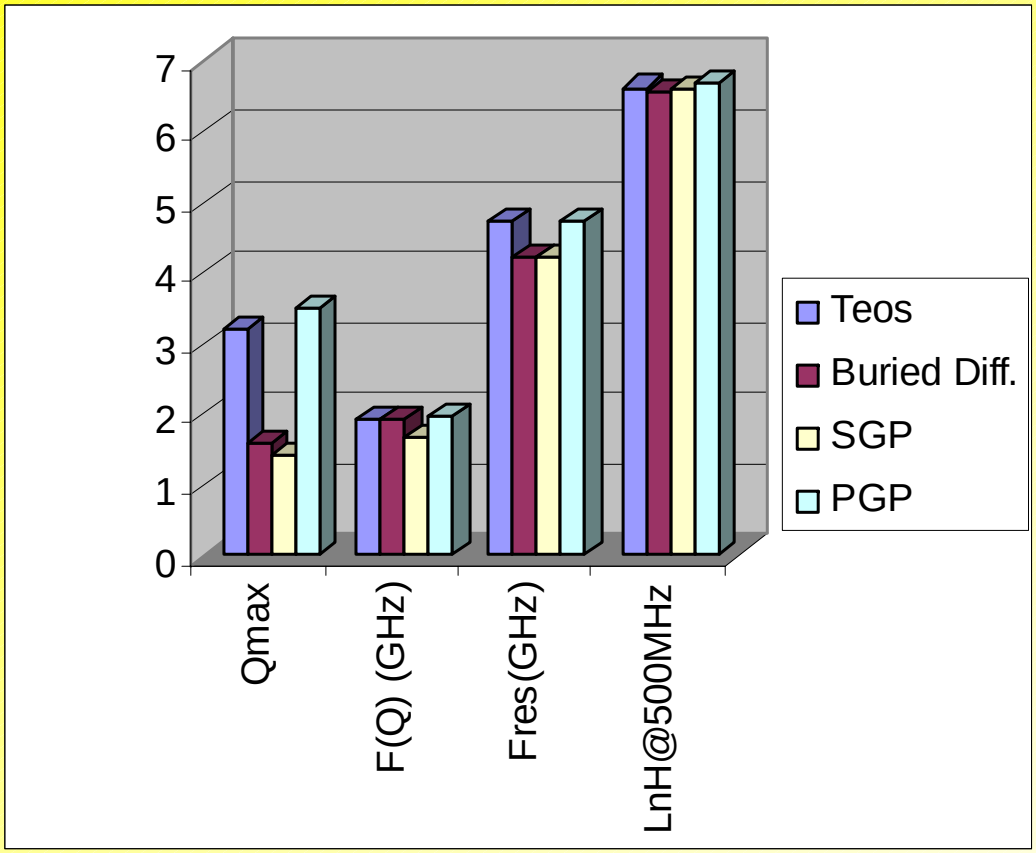
Comparison of Inductor Measurents for No GP, Diffused GP, SGP and PGP



W = 12 µm, S = 6 µm, n = 4

- **Qmax reduces by 55% with inclusion of SGP**
- **L values effectively remain constant**
- **Introducing a PGP results in a slight improvement of Qmax**

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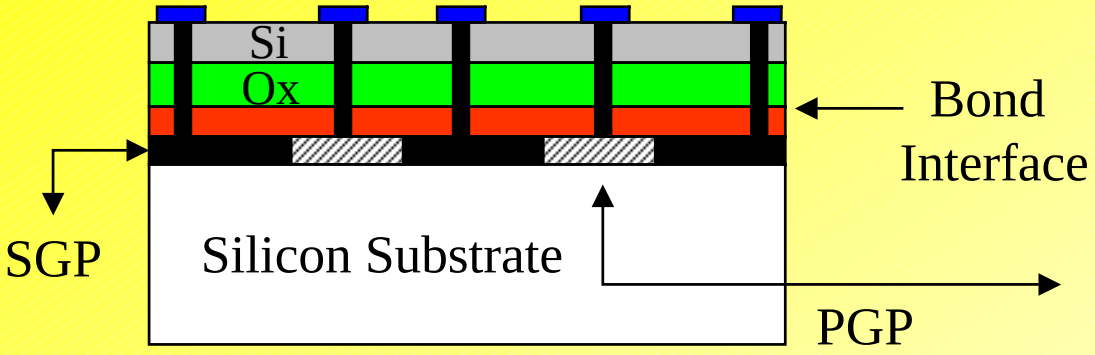
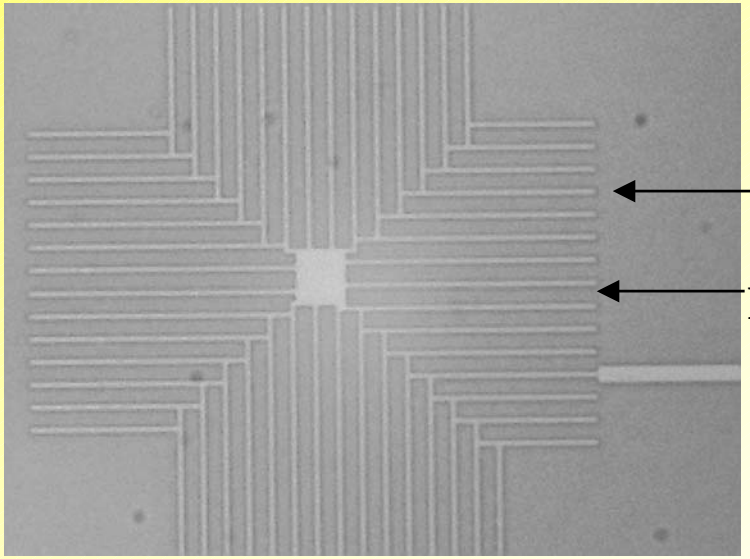
Incorporation of PGP into GPSOI





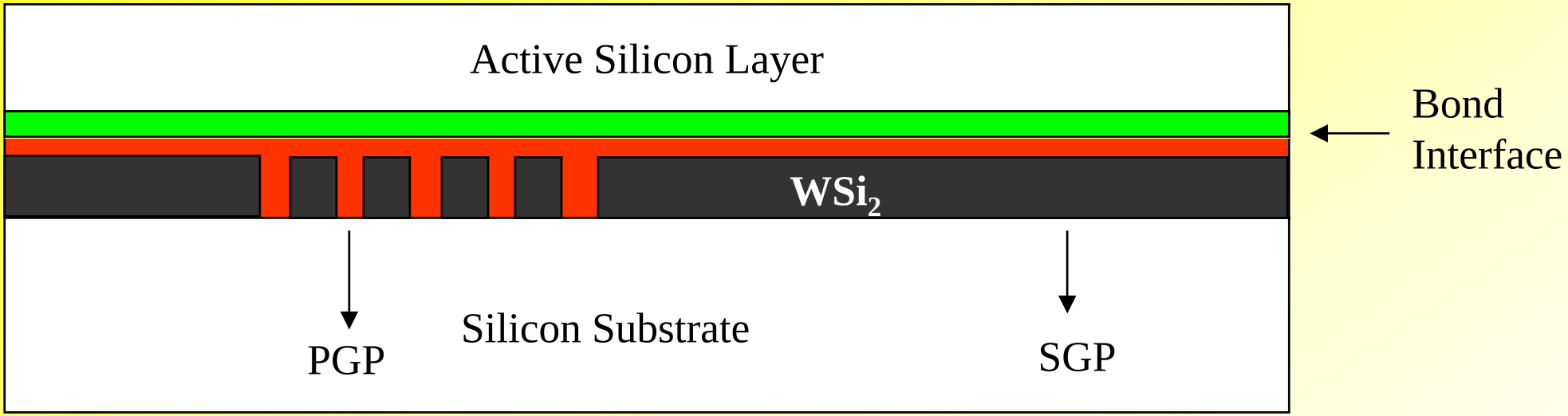
Integration of Patterned areas and solid areas on the same substrate.

Yue et al: IEEE Journal of Solid State Circuits Vol. 33 No. 5 May 1998

Planarisation Issue

- Distance between two WSi_2 fingers must be less than 100 µm. In this case: 8 µm
- Polysilicon deposition
- Chemical mechanical polishing.- Producing surface suitable for bonding.

Process Sequence for Incorporation of PGP and SGP on same substrate



1. LPCVD of WSi. Selective patterning of GP leaving PGP and SGP regions.
2. LPCVD of Polysilicon. (>0.8µm)
3. CMP of polysilicon leaving a planarised bondable surface. Polysilicon(0.2 µm).
4. Bonding of planarised polysilicon layer to oxidised active substrate.
5. Post bond Anneal 1050C 2 hrs
6. Grind and polish to required active layer thickness.

Conclusions

GP PROCESS INTEGRATION

- WSi_2 can be readily integrated into SOI process:
    - Require CMP of a Polysilicon layer.
    - Polysilicon to oxide bond
- For GPSOI substrates WSi_2 can be used in contact Via refill.

GPSOI AND CROSS-TALK

- Top-Down contact to GP using WSi_2 in Via refill.
- WSi_2 employed in Faraday cage structure creating an enclosed metal cage.
- GP greatly reduces noise between Tx and Rx.
    - At 1GHz 35dB improvement in noise for WSi_2 GP only, over control SOI.
    - At 1GHz 70dB reduction in noise for Faraday cage over the SOI control.

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Conclusions

GPSOI AND INDUCTANCE

- Introduction of GP results in a reduction of inductor Quality Factor.
    - 55% reduction in Q.
- Employing a patterned GP structure results in no loss of inductor Quality Factor.
    - Slight improvement of Q.
- Integration of SGP and PGP on the same Die/Substrate requires trench refill and planarisation.