**PhD Project Proposal**

School of Electronics, Electrical Engineering and Computer Science

& ECIT Global Research Institute

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| **Proposed Project Title:** **Energy-Quality Scalable Processors based on Data Mining**  |
| **Principal Supervisor: Dr. Georgios Karakonstantis**  |
| **Keywords:** Approximate Computing, Data Mining, Computer Architecture, Low Power Design, Dependability, FPGAs **Project Description:** Currently, manufacturers go to great lengths to guardband the manufactured hardware against any potential functional failure induced by the highly unreliable and dynamically varying nanometer silicon. Existing measures may have accomplished to hide any inaccurate hardware behaviour from the software layers and maintain acceptable yield levels, but unfortunately the large energy, performance, and area overheads that they incur limit their viability. The incurred overheads have urged research community to look for alternative computing paradigms in which even inaccurate computation and approximate storage could be accepted and any quality loss could be traded off for energy gains. Although existing studies may have shown the benefits of such a paradigm in a variety of application domains there is still a need for the integration of schemes for providing minimum quality guarantees under various operating conditions. The primary aim of this project is to investigate schemes based on data mining for minimizing at low cost the impact on system operation of any potential online failure that may be induced randomly. The inherent error resilience and certain statistical characteristics of various applications will be exploited for achieving adequately-reliable and energy efficient operation, while limiting or even avoiding the penalties incurred by traditional approaches. The developed mechanisms will also consider the use of approximate arithmetic units and caches/memories, which may help to save energy but be the source of deterministic errors the impact of which will also be minimized. The developed schemes will be integrated on a RISC-V processor and could be ported on a FPGA and evaluated with a variety of popular multimedia and data-mining applications. Overall, the proposed framework will allow the adaptation of any system to dynamically changing operating conditions and user requirements and is expected to be beneficial for a variety of application domains from embedded to high-performance systems.  The PhD studentship will be based at the Data-Science and Scalable Computing Centre (DSSC) of the Queen’s Global Research Institute of Electronics, Communications and Information Technology (ECIT). The PhD student will join a prolific team of PhD students and Research Fellows and extend a successful line of work published recently in top-tier conferences, such as [ISLPED 2018](https://pure.qub.ac.uk/portal/en/publications/variationaware-pipelined-cores-through-path-shaping-and-dynamic-cycle-adjustment-case-study-on-a-floatingpoint-unit%28c712649d-2144-498e-a175-9e9e043a5d85%29.html) and [IOLTS 2018](https://pure.qub.ac.uk/portal/en/publications/minimization-of-timing-failures-in-pipelined-designs-via-path-shaping-and-operand-truncation%280e2ca242-8a05-4c5e-b265-4b43fc39f6b5%29.html).  |
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