**PhD Project Proposal**

***School of Electronics, Electrical Engineering and Computer Science***

***& ECIT Global Research Institute***

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| **Proposed Project Title:** **Intelligent Memory Access Pattern Scheduling for Power and Performance Optimization**  |
| **Principal Supervisor: Dr. Georgios Karakonstantis Second Supervisor: Dr. John McAllister** |
| **Project Description:** The explosive growth of generated data by the increasing number of connected devices and the resultant need for more memory capacity is driving the aggressive scaling of Dynamic Random- Access Memories (DRAM). However, aggressive DRAM scaling is hampered by the need of periodic refresh cycles to retain the stored data, the frequency of which is conventionally being determined by the worst case retention time of the weakest cells. Such an approach might guarantee error free storage but its viability is questionable due to the incurred large power and performance overhead that may reach up-to 25-50% in future densities. However, our recent work has shown that conventional high refresh rates may not be required due to extremely low occurrence of the assumed worst-case scenarios, or due to the implicit refresh operation that occur during every memory access, a feature that has not yet been studied in depth. This project aims at exploiting the implicit refresh incurred by each memory access for relaxing the refresh rate, while minimizing the resulting memory errors. This will be achieved by modifying algorithmic parameters that influence the access patterns such that all stored data are being touched within a target time interval that is necessary for meeting a target error rate. The proposed method will be applied on popular algorithms used in image processing and data mining and the power and performance gains will be evaluated on a commodity server or an FPGA using a high level programming model.  The PhD studentship will be based at the DSSC Centre of the Queen’s Global Research Institute of Electronics, Communications and Information Technology (ECIT). The PhD student will join a prolific team of PhD students and Research Fellows and extend our prior work ([IOLTS 2017](https://pure.qub.ac.uk/portal/en/publications/relaxing-dram-refresh-rate-through-access-pattern-scheduling-a-case-study-on-stencilbased-algorithms%2834267f22-79a9-4969-990c-86d5e92f186a%29.html)). |
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